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TO:	FROM:
Mail Stop Amendment	Morgan Malino 408-737-7200 @ 114
COMPANY:	DATE:
PTO	DECEMBER 23, 2004
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PHONE NUMBER:	RE:
703-308-4357	See Below

URGENT FOR REVIEW PLEASE COMMENT PLEASE REPLY PLEASE RECYCLE

NOTES/COMMENTS:

Docket #	UNITY P035	By	MEM	Faxing Date	December 23, 2004
Ser. No:	10/605,757	Filing Date:	10/23/2003	Inv(s)	Rinerson et al.
Title:	Multi-Layer Conductive Memory Device				

The following is being transmitted to the U.S. Patent Office:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: RINERSON et al.

Attorney Docket No.: UNTYP035

Application No.: 10/605,757

Examiner: Tu Tu Ho

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Filed: October 23, 2003

Group: 2818

DEC 23 2004

Title: Multi-Layer Conductive Memory Device

Confirmation No.: 2756

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being transmitted by facsimile to fax number 703-872-9306 to the U.S. Patent and Trademark Office on December 23, 2004.

Signed: _____
Patty Lomeli**RESPONSE TO ELECTION/RESTRICTIONS**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Ms.:

In response to a Restriction Requirement mailed November 24, 2004, Applicant elects claims 1 – 32 of group I and withdraws claims 33 – 45 of group II, with traverse.

As an initial matter, the Examiner has identified claim 33 as a linking claim. It is the understanding of the undersigned that a linking claim should not be associated with a group since such claims must be examined with any of the linked inventions that might be elected.

Additionally, the Examiner stated, "[T]he process in claim 33 could be used to make a contact for a nonvolatile conductive memory element having a pair of source/drains, a floating gate, and a control gate, the contact comprising bottom and top conductive metal oxide layers, the bottom conductive metal oxide layer stacked upon the control gate, and the resistance of the conductive memory element can be modified during operation to store information by applying a suitable voltage potential across the floating gate and the control gate, which is different from a conductive memory device comprising a bottom (first) conductive metal oxide layer stacked upon a first electrode as recited in claim 1 or claim 27 of Invention I."

The undersigned is not able to follow the Examiner's logic and respectfully requests a clarification. Specifically, the undersigned is not clear as to how the Examiner considers "depositing onto the bottom conductive metal oxide layer a top conductive metal oxide layer" (claim 33) is different from "a second conductive metal oxide layer stacked upon . . . the first conductive metal oxide layer" (claim 27). At this time the undersigned does not wish to take a position as to whether the two claims are different, but simply would like clarification of the Examiner's position regarding the differences.

Applicant believes that the above is fully responsive to the Restriction Requirement. If for any reasons the Examiner believes a telephone conference would in any way expedite resolution of any pending issues, the Examiner is invited to telephone the undersigned.

Respectfully submitted,
UNITY SEMICONDUCTOR CORPORATION



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